IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) A method for recording segment execution times in a processing system, the method comprising the steps of:

~~recording a timestamp~~ writing a location for storing a timestamp corresponding to the beginning of a segment to be executed, the recording step being conducted through a firmware operation; and

updating the location for storing the timestamp with an elapsed segment execution time, the updating step being conducted through a plurality of hardware based operations autonomously, without firmware interaction, ~~wherein the plurality of hardware based operations are executed without firmware interaction.~~

2. (Original) The method of claim 1, wherein the recording step comprises writing a first memory address into a globally accessible timestamp address register.

3. (Original) The method of claim 1, wherein the updating step comprises:

reading the contents of a second memory location designated by an update address register;

writing the contents of the second memory location into a location value register;

adding the elapsed segment execution time to the location value register contents; and

storing the location value register contents to the second memory location indicated by the update address register.

4. (Original) The method of claim 3 further comprising the steps of:

clearing the elapsed segment execution time stored in an elapsed time register; and

setting a second value in the update address register with a first value from a timestamp address register.

5. (Original) The method of claim 1 further comprising the step of initializing hardware components of the processing system, the initializing step further comprising the steps of:

disabling timestamp assist functions;
setting an elapsed time register to an initial value;
writing an initial address into a timestamp address register;
writing the initial address to an update address register; and
enabling the timestamp assist functions.

6. (Original) The method of claim 1 further comprising the step of invoking an interrupt handler if a second segment is received for processing during the updating step.

7. (Original) The method of claim 6, wherein the step of invoking an interrupt handler further
comprises:

generating an interrupt signal in a memory controller;
determining if the updating step is still in process;
determining if a timeout has been reached if the updating step is determined to still be in process;

restarting the updating step for the second segment; and
clearing the interrupt signal from the memory controller.

8. (Original) A method for recording segment execution times through a central processing
unit, the method comprising the steps of:

writing a first determined memory address into a timestamp address register with a firmware based operation;

reading contents of the first determined memory address into a location value register with a hardware based operation;

adding an elapsed time value corresponding to a segment execution time to the contents read into the location value register to create an updated value, the adding step being conducted with a hardware based operation; and

storing the updated value to the first determined memory address with a hardware based operation.

9. (Original) The method of claim 8, wherein the reading step comprises:

reading a memory location from an update address register in a timestamp assist logic module; and

writing the memory location into the location value register in the timestamp assist logic module.

10. (Original) The method of claim 8, wherein the adding step comprises:

reading the elapsed time value from an elapsed time register in a timestamp assist logic module, the elapsed time value corresponding to an elapsed time between a start of a segment execution and the step of reading the elapsed time; and

adding the elapsed time value to the contents stored in the location value register.

11. (Original) The method of claim 8, wherein the storing step comprises:

reading the contents of a location value register; and

writing the contents read from the location value register to the first determined.

12. (Original) The method of claim 8 further comprising the steps of:

generating a segment processing interrupt when a second segment is received for processing during one of the writing, reading, adding, and storing steps;

transmitting the segment processing interrupt to a processor;

interrupting segment processing; and

invoking a timestamp busy interrupt handler.

13. (Original) The method of claim 12, wherein invoking the timestamp busy interrupt handler
comprises:

determining if the updating step is still in process;

determining if a timeout has been reached if the updating step is determined to still be in process;

restarting the updating step for the second segment; and

clearing the interrupt signal from the memory controller.

14. (Currently Amended) An apparatus for recording segment execution times in a processing system, the apparatus comprising a memory controller in communication with a central processing unit and a memory, the memory controller comprising:

at least one control register;

at least one address register; and

a timestamp assist logic module configured to conduct timestamp update operations autonomously from the central processing unit by automatically updating a memory location specified by a value in the address register without interaction with the central processing unit.

~~wherein the memory controller is configured to conduct timestamp update operations autonomously from the central processing unit.~~

15. (Original) The apparatus of claim 14, wherein the timestamp assist logic module comprises:

an elapsed time module;

an update address register; and

a location value register.

16. (Original) The apparatus of claim 15, wherein the elapsed time module comprises an elapsed time register having an updated elapsed time value stored therein.

17. (Original) The apparatus of claim 14 further comprising:

a processor bus in communication with the central processing unit and the memory controller for communication therebetween;

a memory bus in communication with the memory and the memory controller for communication between the memory controller and a plurality of memory locations in the memory; and

a system bus in communication with the memory controller, the system bus being configured to connect one or more additional devices to the memory controller.

18. (Original) The apparatus of claim 14, wherein the control register is configured to generate an interrupt signal when the timestamp assist module receives a second segment for processing while a first segment is currently processing, the interrupt signal being transmitted to the central processing unit via a system bus.

19. (Currently Amended) A memory controller for recording segment execution times in a complex processor system, the memory controller comprising:

a timestamp assist logic module; and

~~a timestamp control module;~~

a timestamp address module, wherein an operating system of the complex processing system may write a value specifying a location in a memory where a timestamp will be stored; and ~~wherein the memory controller~~ the timestamp assist logic module is configured to ~~communicate with a the memory~~ write to the specified location in order to execute a timestamp update operation corresponding to a particular segment execution time, the timestamp update operation being conducted without interaction with ~~an~~ the operating system of the complex processing system.

20. (Original) The memory controller of claim 19, wherein the timestamp assist logic module comprises:

an elapsed time module;

an update address module; and

a location value module.

21. (Original) The memory controller of claim 20, wherein the elapsed time module comprises a device for calculating and storing an elapsed time value corresponding to the time elapsed between initial segment execution and completion of segment execution.

22. (Original) The memory controller of claim 20, wherein the elapsed time module comprises an elapsed time register having an updated elapsed time value stored therein.

23. (Original) The memory controller of claim 19 further comprising:

a processor bus in communication with the operating system and the memory controller for communication therebetween;

a memory bus in communication with a plurality of memory locations in the memory and the memory controller for communication therebetween; and

a system bus in communication with the memory controller for communication between the memory controller and additional devices in the complex processing system.

24. (Original) The memory controller of claim 19, wherein the timestamp control module is configured to generate an interrupt signal when the timestamp assist logic module receives a second segment for processing while a first segment is currently processing, the interrupt signal being transmitted to a central processing unit.